In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Previously Presented) A method of performing a dot product operation with rounding and shifting in a microprocessor in response to a single rounding dot product instruction, the method comprising the steps of:

fetching a first pair of elements and a second pair of elements;

forming a first product of the first pair of elements and a second product of the second pair of elements;

combining the first product with the second product to form a combined product and rounding the combined product to form an intermediate result via an arithmetic circuit having a first input receiving said first product, a second input receiving said second product and a carry input to a mid-position receiving said rounding value to form the intermediate result; and

right shifting the intermediate result a selected amount to form a final result.

Claims 2 and 3. (Canceled)

4. (Previously Presented) The method of Claim 1, wherein the rounding value is 2^n and the selected shift amount is n+1.

5. (Original) The method of Claim 4, wherein n has a fixed value of fifteen.

Claims 6 to 9. (Canceled)

10. (Original) The method of Claim 1, wherein the step of combining comprises subtracting the product of second pair of elements from the product of first pair of elements.

11. (Original) The method of Claim 1, wherein the step of combining comprises adding the product of second pair of elements to the product of first pair of elements.

12. (Canceled)

13. (Previously Presented) A digital system having a microprocessor operable to execute a rounding dot product instruction, wherein the microprocessor comprises:

storage circuitry for holding pairs of elements;

a multiply circuit connected to receive a first number of pairs of elements from the storage circuitry in a first execution phase of the microprocessor responsive to the dot product instruction, the multiply circuit comprising a plurality of multipliers equal to the first number of pairs of elements;

an arithmetic circuit having a plurality of inputs each connected to receive a corresponding one of the plurality of products from the plurality of multipliers and a mid-position carry input for mid-position rounding responsive to the rounding dot product instruction; and

a shifter connected to receive an output of the arithmetic circuit, the shifter operable to shift a selected amount in response to the rounding dot product instructions.

Claims 14 to 24. (Canceled)